Title: Digital Logic Design

Code Number: EE2102

Credit Hours: 3 (3+1)

Prerequisites: MD1102 Computer Hardware Engineering

Semester: 3rd

Course Objectives

The course will enable students to:

1. Solve binary systems and Boolean algebra, including number systems and conversions, arithmetic operations, postulates, theorems, and functions.
2. Apply digital logic circuits using basic logic gates, ensuring proficiency in theoretical concepts
3. Analyze the operational characteristics and performance of combinational logic circuits, sequential circuits and advanced circuits
4. Perform experiments on HDL and simulation tools to simulate and verify digital logic circuits prior to their hardware implementation.
5. Demonstrate the functionality and performance of designed digital circuits through practical experiments and measurements using lab instruments.

Contents

Unit 1: Binary Systems

1. Introduction
2. Number Systems and Conversions
3. Arithmetic with number systems
4. Signed and unsigned number systems and their arithmetic Binary Codes

Unit 2: Boolean Algebra & Logic Gates

1. Boolean Postulates & Theorems
2. Boolean Functions and their Complements
3. Sum of Min Terms & Product of Max Terms
4. Standard forms & Canonical Forms
5. Digital logic gates

Unit 3: Combinational Logic

1. Analysis and Design
2. Code Converters
3. Adders & its types
4. Subtractors, Multiplier
5. Magnitude Comparator
6. Decoders and Encoders
7. Multiplexers
8. Combinational Logic using Verilog simulation

Unit 4: Sequential Circuits

1. Latches (SR Latch, D Latch)
2. Flip Flops (D Flip Flop, JK Flip Flop, T Flip Flop)
3. Characteristic Tables, Characteristic Equations.
4. Design and Analysis of Clocked Sequential Circuits (State Equations, Tables & Diagrams)

5. Designing Counters

Unit 5: Registers & Counters

1. Simple registers
2. Registers with parallel Load
3. Shift Registers/Serial to parallel Convertors
4. Universal Shift Register
5. Asynchronous and Synchronous Counters
6. Ripple, Binary, BCD, & Johnson Counters
7. Verilog for sequential logic

Unit 6: Introduction to Arithmetic Logic Units

1. Simple Arithmetic Logic Units (ALU)
2. Introduction to FPGA

Lab Work Outline

Hardware: Demonstrate the students with the Combinational Digital Logic Design and Sequential Digital Logic Design through the implementation of Digital Logic Circuits using ICs of basic logic gates and some simple digital logic circuits.

Software: Familiarization with HDL (Verilog). To get the students acquainted with the HDL based Digital Design Flow. Use of other tools like Logisim / Proteus for the analysis of logic circuitries prior to their hardware implementation.

Teaching-Learning Strategies:

The pedagogical approach to this course relies on face-to-face teaching in a university classroom environment. The lectures are delivered using multimedia support and on white board. Students are engaged and encouraged to solve real world problems using computer-aided tools.

Assignments/Types and Number with calendar:

A minimum of four assignments to be submitted before the written exams for each term.

Assessment and Examinations:

Sr. No.	Elements	Weightage	Details
1.	Midterm Assessment	35%	It takes place at the mid-point of the semester.
2.	Sessional Assessment	25%	It is continuous assessment. It includes classroom participation, attendance, assignments and presentations, homework, attitude and behavior, hands-on-activities, short tests, quizzes etc.
3.	Final Assessment	40%	It takes place at the end of the semester. It is mostly in the form of a test, but owing to the nature of the course the teacher may assess their students based on term paper, research proposal development, field work and report writing etc.

Recommended Books:

1. Morris Mano and Charles R. Kime, "Logic and Computer Design Fundamentals", Prentice Hall. Latest Edition
2. M. Morris Mano and Micheal D. Ciletti, "Digital Design with an introduction to the Verilog HDL", Prentice Hall, 5th Edition.
3. Tocci and Widmer, "Digital Systems: Principles and Applications". Prentice Hall. Latest Edition